Fast Detector Readout for the HADES-RICH ◇

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The dilepton spectrometer HADES currently under construction at the GSI requires new concepts for detector readout and data aquisition [1]. The expected high interaction rate and the need for a fast and very effective background suppression lead to the main design criteria for the detector readout electronics. These are the maximum processing time of $10\mu s$ per event and the use of a multilevel trigger system for online data reduction.

Two modules were developed for the lepton-identifying RICH detector [2]: A preprocessing frontend module (PFM) and a VME based readout controller (RC). The PFM is a multi channel data aquisition system on a small PCB that can be mounted directly to the detector. All main components of such a system are implemented in the PFM: 64 charge sensitive preamplifiers, shapers, track&hold-stages, ADC, digital discriminator, zero suppression and memory for event data. The number of channels can be increased by cascading modules using a mixed parallel and daisy chained readout bus. In fig. 1 the layout of the module and the location of the main components are shown.

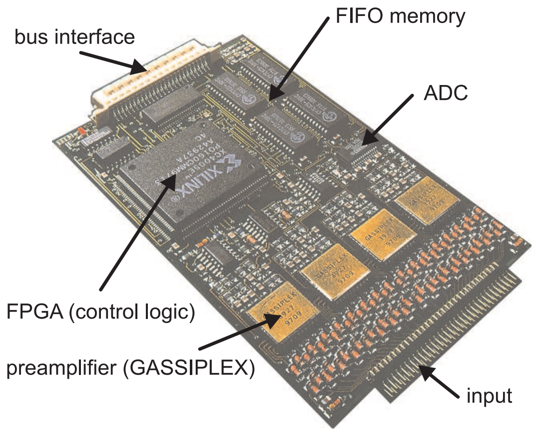

Fig. 1: Layout and main components on the PFM; all components besides the 64-pin input connector are mounted in SMD technology

The 64 inputs are sensitive for positive signals up to 300 fC ($\simeq$ 6.5 MeV Si) and are protected against positive spikes by low leakage-current diodes. The analog signal processing is done by four GASSIPLEX ASICs developed at CERN [3]. Their outputs are connected to a 20×10^6 samples/s half-flash-ADC via a fast video multiplexer. The resulting 10 bit binary data word is processed in a pipelined logic inside a reprogrammable field programmable gate arry (FPGA), that performs a zero suppression, adds a channel number to each data word and generates a hit pattern for 64 input channels. The valid data words are written to one FIFO memory, the hit pattern is transferred to a second FIFO memory. Because of the pipelined operation and the usage of memories on the module one PFM is able to buffer about 15 events at full coverage of all input channels. The configuration of the PFM and the data readout are done by access cycles on the digital bus interface of the PFM, that are controlled by a special readout controller.

This VMEbus based module is the interface between the PFM and the central data aquisition. Its four PFM-ports are used to connect up to 16 PFMs. The ADC-values stored on the PFM are read out and written to a memory on the RC while the hit pattern is directly transferred to a special interface without any processing. To reduce latency times the memory consists of two switchable banks of 128 k $\times$ 32 bit SRAM. One is written to from the detector side and the other one is read out via the VMEbus interface, which is capable of transferring data in the fast block transfer mode. All readout and control cycles on the RC are either generated by fast FPGAs to achieve the requirements of 10 μs for a complete readout [4] or can be simulated by software for test purposes.

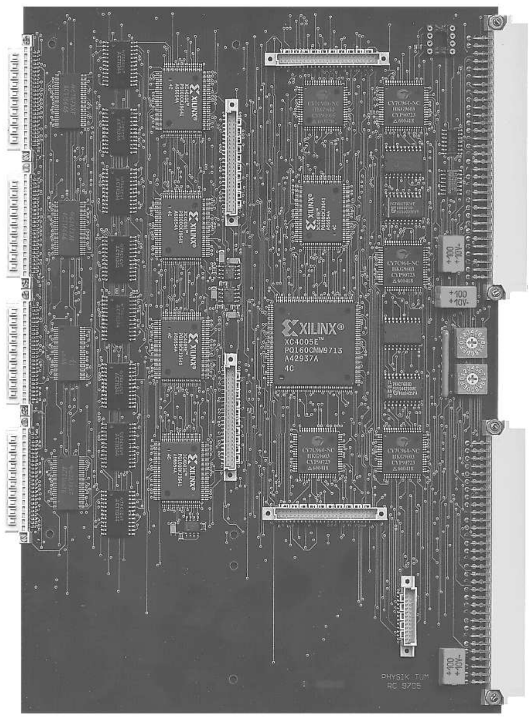

Fig. 2: Layout of the RC. The double height eurocard $233 \times 160\,\mathrm{mm}^2$ can handle up to 1024 channels.

References

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Eine schnelle Auslesesteuerung für den Photonendetektor im HADES-RICH

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