Status of the DAQ System of the COMPASS Experiment

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COMPASS is a new fixed target experiment under construction at the CERN Super Proton Synchrotron (*SPS*) aimed at the study of structure and spectroscopy of hadrons with multiple types of high intensity beams [1].

The apparatus of COMPASS will have 250,000 channels which are read out by a fast data acquisition system with minimum deadtime. At a trigger rate of 10 – 100kHz and an event size around 30 kBytes a data rate of 600 MBytes – 6 GBytes per SPS spill is reached leading to 300 TBytes of data per year on tape. Our group at TUM is responsible for the development of the data acquisition system (DAQ).

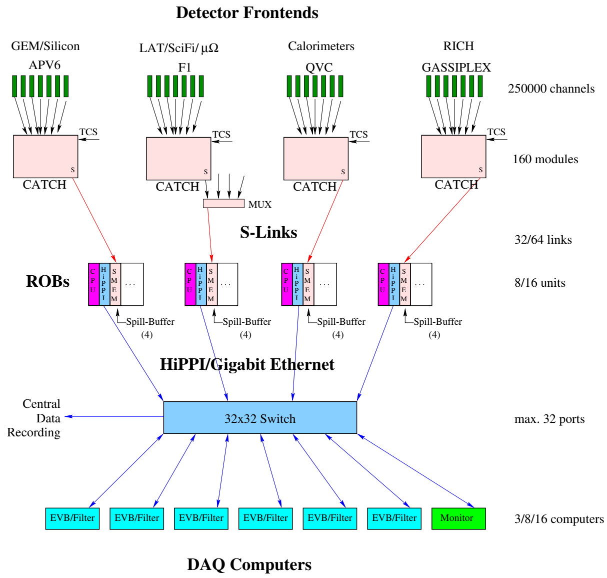

Fig. 1: The COMPASS DAQ system

Overview. The mostly pipelined detector readout electronics feeds the data in concentrator boards in VME called *CATCH*, which are developed at the University of Freiburg. From these boards the data is then transfered via optical links to the DAQ computers. These links follow the *S-link* standard [2] developed at CERN. It specifies a protocol and a connector (IEEE 1386, CMC) for a data transfer link. The actual transmission can be accomplished by different types of physical interfaces. In COMPASS we use a FibreChannel version of S-link which achieves up to 100 MByte/s per link via optical fibres.

The DAQ system makes use of the accelerator cycle of a 2.4 s long beam extraction every 14.4 s (*spill*). This allows to buffer the data created by physical interactions in the experiment and transmit it at a lower continuous rate. The destination of the S-links are PCI cards called *spill buffers* which receive the data and store it in an onboard SDRAM memory. The computers in which these PCI cards are installed are server type high performance PCs with two processors and two PCI buses. While one PCI bus hosts the spill buffers the other contains a Gigabit Ethernet interface card. This effectively reduces the number of data transfers per PCI bus. The Gigabit Ethernet network connects the buffer computers to eventbuilder computers, where the data blocks of different detectors are assembled to complete events.

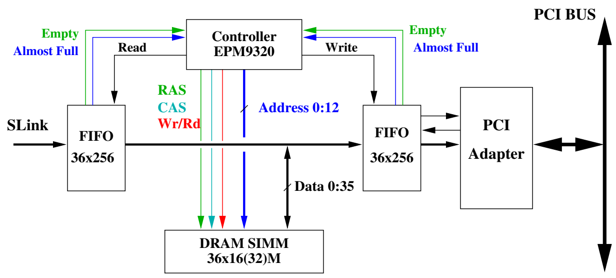

Fig. 2: The scheme of the spill-buffer card

Spill-buffer. The spill-buffer card, which was developed at TU Munich, has on one side an S-link receiver interface and on the other side a PCI interface. To the S-link interface the physical link can be plugged, e.g. a FibreChannel card with optical link. As PCI interface the chip AMCC 5933 is used which implements sufficient functionalities for our purposes and is addressed by the host computer via the internal PCI bus. The two interfaces are logically connected by a large FIFO memory of 64 MBytes. Technically this is achieved by means of a DRAM memory with some control logic making it appear as a FIFO. The board has been successfully used at several testbeams to read out silicon detectors and CATCH prototypes. A newer version implementing faster SDRAM memory is under design in winter 1999/2000.

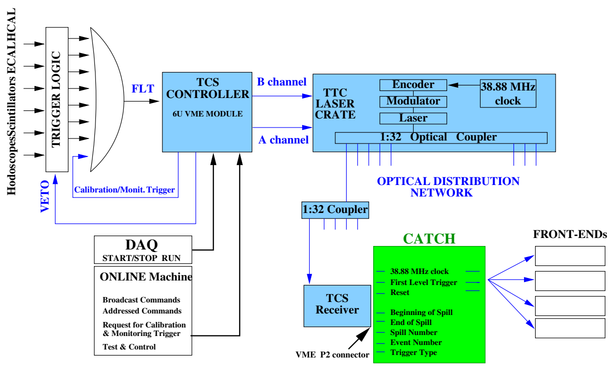

Fig. 3: The COMPASS trigger control system TCS

Trigger Control System. To insure data integrity in the pipelined readout architecture each trigger has to be labeled by a unique event number. The synchronous transmission of the trigger and its identification to all detectors is done by means of optical signals encoded by the Trigger Control System (*TCS*).

The TCS controller, a 6U VME board, receives its input from the trigger logic which forms the decision on valid events on the base of scintillator and calorimeter signals. In addition to physical triggers it also accepts requests for calibration and monitoring triggers for which a pre-signal preceding the special trigger by a defined time can be generated to gate e.g. test pulsers or LEDs.