First Experiences with the HADES-RICH Readout Electronics ◇

M. Böhmer, A. Elhardt, J. Friese, R. Gernhäuser, H. Gilg, J. Homolka, A. Kastenmüller, H. J. Körner, D. Maier, and M. Münch

The RICH in the dilepton spectrometer HADES [1] is designed for fast and effective lepton identification. A 2-dimensional position measurement of Cherenkov photons is performed in a gaseous photon detector (28 272 pads) with 10 bit pulse height resolution for each channel. The average pad occupancy of ≈ 1% and expected trigger rates up to 100 kHz lead to high data rates. The new readout system for this detector was installed in 1999 and was subject to first in-beam tests.

The readout system consists of two main modules: A preprocessing frontend module (PFM) [2] and a VME based readout controller (RC) [3]. Placed on a small PCB containing 64 charge sensitive preamplifiers, shapers, ADC, FIFO memory and control logic, the PFM performs digitization, zero suppression and pipelined data storage to ensure the multi event capability of the readout.

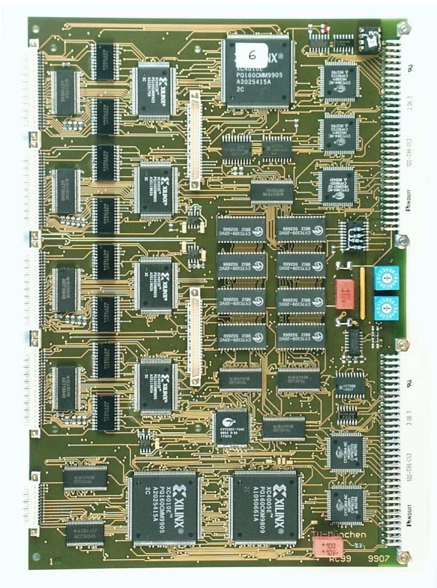

Fig. 1: The new RC module (piggyback PCB removed). Up to 2560 channels are handled by this VME module, controlled by only nine TTL signals

The RC module acts as an interface between the PFMs and the trigger and data acquisition system and concentrates data of up to 40 PFMs before forwarding them to the VME CPU and ATM network.The RC is connected to the central trigger system (CTU) via a detector trigger module (DTU) which implements a complex hardware arbitration scheme. Trigger commands are translated into readout sequences which control the fast transmission of hit patterns from the PFMs through the RC to an image processing unit (IPU). Based on the IPU results (recognised ring) a 2^{nd} level trigger is generated and either initializes the transfer of pad pulse height data from the PFMs to the local RC memory or deletes the data directly in the PFMs. Particular error checking routines ensure a correct assembly of data subsets while each set is complemented with header information and stored. The RC memory is implemented as two banks of 128 k × 32 bit SRAM. This bank structure allows both, data concentration and asynchronous CPU readout at the same time. The banks are entirely switched on DAQ software request such that small latency times can be achieved.

All control logic in the PFM and RC modules is implemented using high density field programmable gate arrays (FPGAs). The modular approach and the high reconfigurability result in a scalable system which is also suitable for the readout of other detector systems without major hardware modifications.

After completion of prototype tests 400 PFM and 15 RC modules were produced and individually checked during the last year. Part of them were then assembled to equip one sector of the RICH photon detector. Noise measurements were performed and proved the correct operation of the ADC system (see Fig. 2). In stand alone mode data transfer rates up to 20 MB/s were measured using VME block transfer.

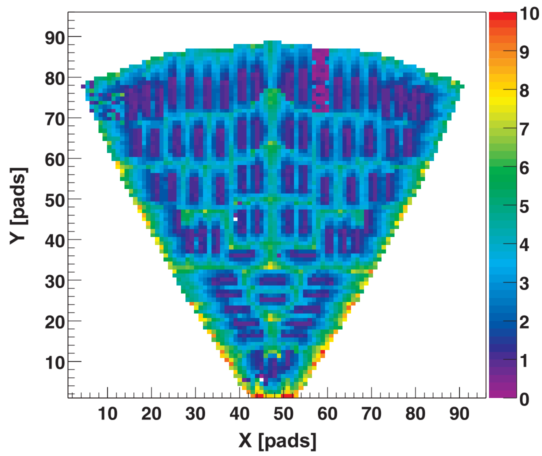

Fig. 2: Pulse heights of noise signals on the RICH padplane. The structure corresponds to the location of PFM connectors and resembles the varying length of pad-to-connector lines.

For beam tests at GSI the system was successfully integrated into the HADES trigger system and DAQ system [4] and operated for the first time in coincidence mode together with the other HADES detectors. First results of these tests are described in [5]). However, in these measurements the design performance could not yet be reached. Meanwhile the full asynchronous readout functionality could be achieved and two photon detectors are presently prepared for the next beam time.

References

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[3] M. Böhmer, diploma thesis, TU München, 1999
[4] M. Münch *et al.*, this report, p.116
[5] M. Böhmer *et al.*, this report, p.95

◇ supported by BMBF and GSI