Sampling ADC Data Acquisition for Multimodality Positron Emission Tomography

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1. Introduction

Multimodality imaging techniques such as combined positron emission tomography (PET) and x-ray computed tomography (CT) have gained increased importance within nuclear medicine. To take advantage of the additional features of magnetic resonance imaging (MRI) a similar combination of PET and MRI is favorable. However, due to the difficult electromagnetic environment within MRI, the PET detector and data acquisition system have to cope with additional interference arising from the MRI system which has to be either shielded appropriately or compensated in the data processing. A modular sampling ADC (SADC) system with online data processing in field programmable gate arrays (FPGAs) was developed for this application and other data acquisition tasks in high energy physics [1]. The system concept was evaluated with PET detectors based on LYSO scintillator crystals and silicon photomultiplier based light detectors [2].

2. The Data Acquisition System

As the basic building block for the DAQ system, a versatile sampling ADC mezzanine card with a size of 70 mm × 130 mm as shown in Fig. 1 was designed. The card includes up to 32 differential analog input channels, which are sampled independently by 12 bit ADCs at sampling rates up to 70 MHz. As the ADCs are available with various sampling rates, the card can be modified to achieve a trade-off between performance and system cost. To attain higher sampling rates, the card can work in an interleaved ADC mode, which can double the maximum sampling frequency to 140 MHz for 16 input channels. To match the incoming analog signals to the ADC impedance, each channel is preceded by a differential operational amplifier (OpAmp). By selecting proper resistor values, the OpAmp circuit can also implement a moderate amplification of the incoming detector signals. For monitoring purposes, the mezzanine sampling ADC (MSADC) provides also 8 independent analog monitor channels, to supervise detector parameters, such as temperature or supply voltage and current.

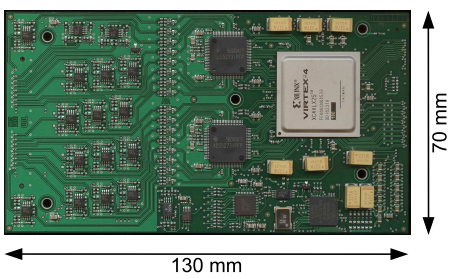

Fig. 1: Mezzanine sampling ADC module

For laboratory setups, the MSADC module can be mounted on a carrier card which provides the supply voltages and access to the analog inputs. A USB interface allows configuration access to the FPGA firmware and data readout. For the integration of higher channel counts, a carrier card in the Advanced Telecom Computing Architecture (ATCA) standard [3] is foreseen, which can hold up to four MSADC modules. Up to 12 carrier cards can then be installed within a 19"-ATCA crate, which allows to integrate up to 1536 channels within one crate. Additionally, the crate may also include further ATCA based processing electronics which can access the acquired data via high bandwidth serial backplane interfaces.

3. FPGA based Signal Processing

The signal processing within the FPGA on the MSADC is divided into two parts. At first, every channel analyzes the incoming data from the continuously sampling ADCs to detect valid detector pulses. If the configured trigger condition is fulfilled, some sampled data points are acquired, marked with a timestamp and stored for further processing. To allow the PET data acquisition during a running MR scan, especially the radio frequency (RF) bursts from the MR scanner (e.g. 64 MHz for a 1.5 T system) must be suppressed by the trigger logic for each channel.

After the trigger decision, the acquired events from all channels are multiplexed and transfered into a single processing pipeline. The processing steps include the determination of the pulse amplitude followed by the reconstruction of a precise pulse time information. The time reconstruction implements a digital constant fraction (CFD) algorithm which provides a time resolution in the order of 1–2 ns, depending on the pulse properties.

A unified interface of the firmware processing blocks allows the easy exchange and migration between different SADC platforms. Fig. 2 shows the coincidence time histogram of two Hamamatsu Multi Pixel Photon Counters (MPPC), acquired with the predecessor of the MSADC system [4] and processed with the same firmware algorithms.

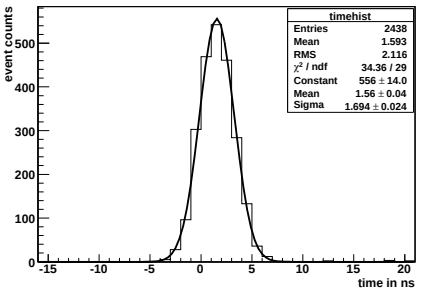

Fig. 2: Coincidence time histogram based on firmware time reconstruction

References

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